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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,419	10/26/2000	Alan McNutt	99 P 7938 US 01	5374

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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	9

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,419	MCNUTT, ALAN	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 12/03/2003.

As indicated in Applicant's response, claims 1-3 have been amended. Claims 1-3 are pending in the office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gates, USPN: 4,969,083 (hereinafter Bates), in view of Narukawa, USPN: 5,978,943 (hereinafter Narukawa); and in view of Lin et al, USPN: 6,026,230 (hereinafter Lin).

As per claim 1, Gates discloses a programmable logic controller (PLC), comprising:

a single chip micro controller (e.g. *CPU 61* – Fig. 3),

a RAM internal to the said single programmable logic controller (e.g. *RAM 14*-- Fig. 1), and

a re-programmable memory internal to the said PLC being used to store the programmable logic controller operating system basic I/O functions (e.g. *BIOS* -- col. 4, lines 6-9; *EEPROM* -lines 46-50; *ROM 65* -- Fig. 3).

But Gates does not specify that the RAM and the re-programmable memory are internal to the single chip micro-controller. However, Gates teaches including the microcontroller functionality and the RAM and EEPROM (Fig. 3) in one input/output scanner unit to correlate

control by the CPU in that scanner unit and the execution/actualization of the PAL control logic (Fig. 3, Fig. 4); hence suggests a tight co-operation of the RAM and re-programmable memory used to execute the PAL logic and control tasks to be encompassed under a same integral body or enclosure. Narukawa, in a method to implement user-customizable programmable logic functionality using a central CPU communicating with peripherals and memory units like Gates, discloses the inclusion of fast memory and ROM storage of re-programmable instructions in a same integrated chip (e.g. *controller 4* – Fig. 1). It would have been obvious for one of ordinary skill in the art at the time the invention was made to implement the one chip controller as taught by Narukawa and incorporate therein all the CPU and memory (volatile and programmable) as suggested by Gates to effect the control and execution of the PLC program logic. One of ordinary skill in the art would be motivated to do so because, if resources are available so it would make it sufficiently feasible without undue expenditure, building a single chip to store all the controlling and storage units as taught by Narukawa, and implement such embodiment to Gates's PLC system would enable all the functional elements needed to run and debug the PLC program as taught by Gates to be located in one place, making thereby the process of tracking malfunction and actualizing the user-defined implementation much less prohibitive and/or more resource-efficient as suggested by Narukawa (col. 1, lines 17-34)

Nor does Gates expressly specify that the re-programmable memory is operable to actualize the PLC functions. Gates does disclose a *logic scanner 57* with programmable array logic functionality (e.g. *PAL 81* --Fig. 3; col. 5, lines 1-16) along with the EEPROM storing basic operating system of the PLC (*ROM 65* (Bios) – col. 4, lines 30-37). Reminiscent to the functions of the PAL and the logic scanner which are operable in conjunction with the EEPROM

(BIOS) to control the actualization of the PLC functions as suggested by Gates (e.g. Fig. 3), a simulation system as taught by Lin, using FPGA analogous to the PAL to actualize a circuit design with software simulation thereof, is disclosed with the use of EEPROM to store the configuration data (e.g. *EEPROM 704* --Fig. 22; *configuration data* -- col. 59, lines 26-46) for programming the FPGA via an user program. It would have been obvious for one of ordinary skill in the art at the time the invention was made to improve the EEPROM contents of Gates' PLC so to include therein not only the operating system and I/O control data but also the configuration data to actualize the design and control functions of the PLC as suggested via the Gates' PAL, because this would allow such EEPROM configuration data to be subjected to more re-programmable designs induced during the PLC functions actualization or simulation as suggested by Lin.

As per claim 2, Gates discloses a programmable logic controller program for directing a programmable logic controller (PLC), comprising:

a user program (e.g. *ladder program* – col. 1, lines 26-31 – Note: a program edited by means of a personal computer is equivalent to an user configured program); and a system sequencing and coordination instructions necessary (e.g. col. 3, lines 5-28) to operate the PLC,

wherein said user program and sequencing and coordinating instructions are compiled into an executable module, requiring no external operating system (e.g. col. 3, lines 58-61; *compiler task 37* -- col. 5, lines 6-31; Fig. 4 – Note: the compiler task 37 to compile the PLC control program and operable in the executive shell of Fig. 4 at one user computer implicitly discloses requiring no external operating system).

But Gates does not specify the executable is a firmware module, but in view of the teachings by Lin in using re-programmable memory to store configuration data to actualize the programmable circuitry configuration and controller functionality (re claim 1), it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify Gates' method of loading executable into RAM (e.g. col. 5, lines 20-22) so that it would be loading such executable into a ROM as a firmware so to enable a persistent storage of such configuration program, thus facilitating the upgrade or maintenance of such firmware as taught by Lin while keeping an active version thereof in RAM as suggested by Gates.

Nor does Gates specify instructions being compiled into a firmware code of said PLC within a single chip. But this single chip limitation has been addressed above in claim 1 using Narukawa's teaching.

As per claim 3, Gates discloses a program execution device having a re-programmable memory (e.g. col. 4, lines 6-9; *EEPROM* -lines 46-50) and whose function is limited to program execution of the programmable logic controller (e.g. *scanner 55 + logic scanner 57* – Fig. 3); and

a separable communication/programming device (e.g. *PC multi-tasking executive shell* – Fig. 4), which provides the programmability function, wherein such device provides in a separable package all functions required for external communication and conversion of an user program for controlling said PLC from a symbolic form to binary code (e.g. *compiler task 37* - Fig. 4), and

loading of that code in said execution device and wherein said binary code is programmed into memory (e.g. *RAM 85*- col. 5, lines 20-22) of said execution device by direct

manipulation of logic controls of said memory (e.g. col. 5, lines 6-31 – Note: logic stored in RAM in conjunction with scanner logic of Fig. 3 is equivalent to direct manipulation of logic controls configured by code stored in RAM).

But Gates does not specify that the binary code is programmed into the re-programmable memory of said execution device via direct manipulation of controls of said re-programmable memory. In view of Gates' teaching on the configuration logic included in the scanner logic, and Lin's teaching for storing configuration data to manipulate the programmable circuit function of the FPGA as mentioned in claim 1, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify Gates' method as to load into and execute such configuration and logic control code from RAM and adopt Lin' s approach in storing the PLC configuration and operation logic control code in re-programmable memory (e.g. EEPROM) for the same benefits as mentioned in corresponding rejection of claim 2 above.

Nor does Gates specify that the program execution device is limited to executing the PLC within a single chip. But this single chip limitation has been addressed above in claim 1.

Response to Arguments

4. Applicant's arguments filed 12/3/2003 have been fully considered but they either moot in view of the new grounds of rejection or not persuasive. Here are the reasons therefor.

(A) As per independent claim 1 and Applicants' arguments that Gates lack 'internal RAM that is internal... chip micro controller' (Applicants Remarks, pg. 5), it is noted that a new ground of rejection is used to overcome this argument.

(B) As per arguments that Lin does not teach or suggest 'user program and system sequencing instructions ... within said single chip' (Appl. Rmrks, pg. 6, para 3), it is noted that

the single chip limitation has been addressed earlier as mentioned above in claim 1. Because Lin is then used to address only what is lacking in Gates, i.e. a firmware including PLC operating instructions, Applicant's point raised that Lin does not have the 'single chip' limitation which Gates combined with Narukawa has already addressed would be moot or not persuasive.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 6,665,817 to Rieken, disclosing including in one chip programmable logic and memory and DSP.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
January 16, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100